Development of a wet silicon removal process for Replacement Metal Gate and Sacrificial Fin.

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Introduction
The recent development of high k/metal gate has led to the continuity of device scaling and Moore’s law. The Gate last approach (Replacement Metal Gate (RMG)) has been investigated extensively since it enables a broad choice of material to be used, and hence yielding affording better electrical performance [1]. From a wet development point of view, the key step in the RMG approach (figure 1) is the dummy polysilicon removal since it is crucial that no residues remain. This paper will focus first on developing a stable and reproducible process for wet polysilicon removal on 300 mm wafers and secondly on transferring the wet removal process to similar dummy silicon approaches: SiGe RMG and Sacrificial Fin (Sac-Fin). The latter can be seen as a simplified RMG flow (Figure 4).

Experimental
All experiments were conducted on a 300 mm single wafer tool after a Chemical Mechanical Polishing (CMP) step (figure 1, figure 4). As a result, a thin oxide layer may remain in addition to any native oxide having grown on top of the silicon. Since this oxide layer can act as an etch stop layer, a short HF step (0.3%) was given. The timing (20s) was chosen as a compromise between that at which full oxide removal occurs versus minimum loss of Inter-Layer Dielectric oxide (ILD0) which is needed later in the flow for Metal CMP. Silicon removal was performed with tetra methyl ammonium hydroxide (TMAH). The concentration and temperature (5%, 70 °C) were chosen according to the literature, which indicates that high etch rate on polysilicon are obtained at a 5% concentration and a temperature between 70 to 80 °C [2,3]. TMAH process time was set to 6 min in the case of boron implanted RMG patterned wafers (Polysilicon Figure 1) and 1.5 min in the case of Sac-Fin pattern wafers (Amorphous silicon, Figure 4).

Results and discussion
Full poly silicon removal on both PMOS and NMOS 45 nm RMG structure was obtained when the dummy dielectric, i.e. the layer underneath the polysilicon, is SiO2. In the case of SiON, the structures were essentially clean, but residues could still be observed mainly on the NMOS structure (Figure 2). Residues on the corner probably resulted from boron implantation, since boron is known to act as an etch stop layer [4]. Poly silicon residues could also be a result of crystal orientation. Hence XRD analyses were conducted in order to assess crystal orientation difference of polysilicon on top of SiO2 and SiON layers. It was found that crystal orientation could be slightly different and, qualitatively, more <111> polysilicon could be observed in the case of SiON layers. This observation could explain the polysilicon residues on top of SiON layer as it is known that <111> orientations have much lower etch rates [3]. With this in mind, polysilicon etch rate studies on different dummy dielectric are ongoing. The wet silicon process could be transferred as such to other RMG Based flow (SiGe RMG) and could be easily adapted for sacrificial fin approach (Figure 4). The amorphous silicon is also removed by an oxide removal step with HF closely followed by TMAH using the conditions described above. Since no boron doping is involved in the integration flow the process time could be shortened to 1.5 min. As a result 30 nm wide trenches (aspect ratio 3:1) were fully opened. In the Sac-Fins case a full wet approach is more beneficial than the dry approach: TMAH is very selective and cannot etch oxide or the thin TiN layer (5 nm) underneath.

Conclusions
In conclusion we have developed an efficient wet process for polysilicon and amorphous silicon removal with TMAH which is applicable and easily transferable to dummy silicon routes. We are currently investigating processes at a higher temperature such as 80 °C in order to achieve even shorter process times. Other RMG Based flow (SiGe RMG) and could be easily adapted for sacrificial fin approach (Figure 4). The amorphous silicon is also removed by an oxide removal step with HF closely followed by TMAH using the conditions described above. Since no boron doping is involved in the integration flow the process time could be shortened to 1.5 min. As a result 30 nm wide trenches (aspect ratio 3:1) were fully opened. In the Sac-Fins case a full wet approach is more beneficial than the dry approach: TMAH is very selective and cannot etch oxide or the thin TiN layer (5 nm) underneath.

References

Figure 1: High k-last gate-last (RMG) integration flow

Figure 2 Left: RMG opened structure with TMAH with SiO2 dummy dielectric. Right: residues seen after TMAH on SiON dummy dielectric

Figure 3: XRD analysis of Polysilicon on top SiON and SiO2 layers

Figure 4 left: Sac-fin integration flow opened by TMAH. Right: 30 nm Sac-Fin line opened with TMAH.